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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,585	09/29/2003	Nobutaka Kitagawa	243333US2S	1493

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,585	KITAGAWA, NOBUTAKA	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 16* is/are rejected.

7)☐ Claim(s) *2-15 and 17-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/03, 2/17/04,* 6/14/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. ***Claim Objections***

Claim 1 is objected to because of the following informalities:

Claim 1, lines 15-16 recites "connects to each other output nodes". It is unclear what is meant by this claim language. For the purpose of the prior art rejection of claim 1, this phrase is interpreted as "connects in common an output node." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nikutta et a., Patent No. 5,821,804, in view of Liu et al., Patent No. 6,947,267. Nikutta et al. teaches an integrated semiconductor circuit having a semiconductor substrate. With respect to claim 1, an integrated semiconductor circuit further comprises a first electrostatic discharge protection circuit ESD-3 connected between a first external terminal supplied with a first power supply voltage VCC-2 at time of ordinary operation and a first ground terminal VSS-2; a second electrostatic discharge protection circuit ESD-1 connected between a second external terminal supplied with a second power supply voltage VCC-1 at the time of the ordinary operation and a second ground terminal VSS-1, the

second electrostatic discharge protection circuit ESD-1 having substantially the same configuration as that of the first electrostatic discharge protection circuit as disclosed in Col. 4, lines 1-11, and lines 18-24.

However, Nikutta et al. does not disclose a trigger signal line which connects in common an output node of a surge detection circuit of the first and second electrostatic discharge protection circuits, and a common discharge line connected directly to the first ground germinal, connected to the second ground terminal via a parallel circuit composed of a forward-connected parasitic diode element and a reverse-connected parasitic diode element, and used commonly by the first and second of electrostatic discharge protection circuits.

Liu et al. teaches ESD protection circuits for integrated circuits' mixed-voltage interface. Liu et al. teaches an RC circuit 230 used to supply a trigger signal to a transistor 240 that makes use of its internal drain to source parasitic diode element, to accomplish ESD protection as disclosed in Fig. 4. Liu et al. further teaches two of said transistors connected in parallel, the first drawing power from VCC 1 and the second drawing power from VCC 2, each respectively grounded to VSS1 and VSS 2 as disclosed in Col. 5, lines 51-58.

Both teachings are related by being electrostatic discharge protection circuits that are applied to a mixed voltage circuit assembly. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Liu et al., which teaches a parallel circuit composed of two parasitic diode elements, into the ESD protection circuits taught

by Nikutta et al. because due to the voltage levels' difference, the power lines and power pins in the integrated circuits are separated to avoid noise coupling between corrupted and clean buses.

3. With respect to claim 16, an integrated semiconductor circuit further comprises a first electrostatic discharge protection circuit ESD-3 connected between a first external terminal supplied with a first power supply voltage VCC-2 at time of ordinary operation and a first ground terminal VSS-2; a plurality of second electrostatic discharge protection circuits ESD-1 and ESD-2 connected between a corresponding second external terminal supplied with a corresponding second power supply voltage VCC-1 at the time of the ordinary operation and a corresponding second ground terminal VSS-1, each of the second electrostatic discharge protection circuits ESD-1 and ESD-2 having substantially the same configuration as that of the first electrostatic discharge protection circuit ESD-3 as disclosed in Fig. 1. Claim 16 differs from claim 1 by not having a plurality of second electrostatic protection circuits, so the teachings of Nikutta et al. and Liu et al. would apply to reject claim 16.

Allowable Subject Matter

4. Claims 2-5, 14-15, 17-20, and 30-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: Nikutta et al. teaches a first ESD protection circuit, a second ESD

protection circuit, and a plurality of second ESD protection circuits but does not disclose ESD protection circuits comprising a voltage clamp element, a trigger element, and a surge detection circuit. This is not anticipated or rendered obvious by the prior art reference.

5. Claims 6, 9-13, 21, and 24-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: Nikutta et al. teaches ESD protection circuits but does not disclose an ESD protection circuit device comprising an integration circuit connected between the first or second external terminal supplied with a highest potential of those potentials supplied to the first external terminal and the second external terminal and the ground terminal associated with the external terminal supplied with the highest potential, and a trigger bias line connected in common to an output node of the integration circuit and to gates of surge detection elements and trigger elements in the first and second electrostatic discharge protection circuits.

6. Claims 7-8 and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: Nikutta et al. teaches ESD protection circuits but does not disclose

an ESD protection circuit comprising a potential holding circuit connected to the trigger signal line to keep a potential on the trigger signal line at time when a power supply of the circuit device is turned on constant.

7. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: Nikutta et al. teaches a first ESD protection circuit and a plurality of second ESD protection circuits but does not disclose an output of a surge detection circuit of the ESD protection circuit among the plurality of ESD protection circuits that has first detected that electrostatic charge has been applied is supplied to other electrostatic discharge protection circuits via the trigger signal line as a trigger input.

8. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
10/14/2005

PHUONG T. VU
PRIMARY EXAMINER